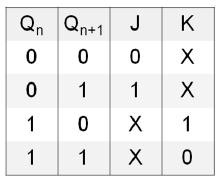
**2 marks answers**

**UNIT – III**

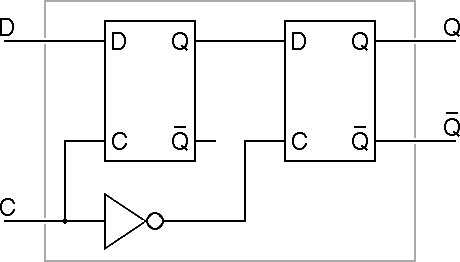
1. State the excitation table of JK Flip Flop.



1. **Write short notes on propagation delay.**

Propagation delay is the amount of time it takes for the head of the signal to travel from the sender to the receiver.

1. **Give the block diagram of master-slave D flip- flop.**



1. **What is ring counter?**

A ring counter is a type of counter composed of a type circular shift register. The output of the last shift register is fed to the input of the first register.

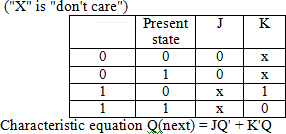
1. **With reference to a JK flip-flop, what is racing?**
2. Because of the feedback connection in the JK flip-flop, when both J & K are equal to 1 at the same time, the output will be complemented while activating the clock pulse.
3. The output is complemented again and again if the pulse duration of the clock signal is greater than the signal propagation delay of the JK flipflop for this particular input combination (J=K=1).
4. There is a race between 0 and 1 within a single clock pulse. this condition of the JK FF is called race-around condition or racing.
5. **What are Mealy and Moore machines?**

Mealy and Moor machines are two models of clocked or synchronous sequential circuit.

**Mealy machine:** The output depends on both the present state of the flip-flops and on the inputs.

**Moore machine:** The output depends only on the present state of the flip-flops.

1. **Write the characteristic table and equation of JK flip flop.**

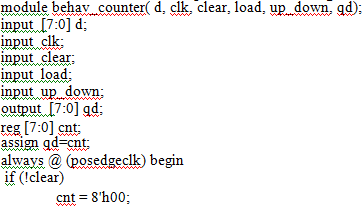


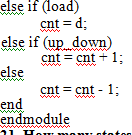
1. **Write any two applications of shift registers.**

(i)Parallel to serial conversion for signal transmission

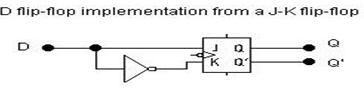
(ii)Pattern recognition

1. **Write the HDL code for up-down counter using behavioral model.**

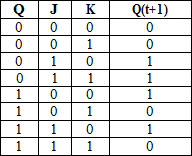




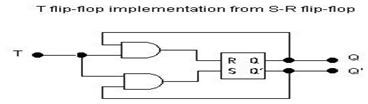
1. **Show D flip-flop implementation from a J-K flip-flop.**



1. **Give the truth table for J-K flip-flop.**



1. **Show the T-Flipflop implementation from SR flipflop.**



1. **What is meant by triggering of Flip flop?**

The state of a flip-flop is switched by a momentary change in the input signal. This momentary change is called a trigger and the transition it causes is said to trigger the flip-flop.

**14. What is a universal shift register?**

(i) A register may operate in any of the following five modes

1. SISO 2. SIPO 3. PIPO 4. PISO 5. Bidirectional

(ii)If a register can be operated in all the five possible ways, it is known as Universal Shift Register

15.Give difference between latch and flip-flop.

|  |  |
| --- | --- |
| **Latch** | **Flip-Flops** |
| Latch has an enable input. | Flip-Flops have a clock signal. |
| As long as enable input is active, the latch output will keep changing according to input. | Flip-flop samples its inputs and changes its outputs only at a particular instant of time i.e., when clock is provided. |

**UNIT – IV**

1. **Define the critical race and non critical race.**

Critical race in asynchronous circuits occur between two signals that are required to change at the same time when the next stable state is dependent on the delay paths in the circuit.

Non Critical race The final stable state does not depend on the change order of state variables.

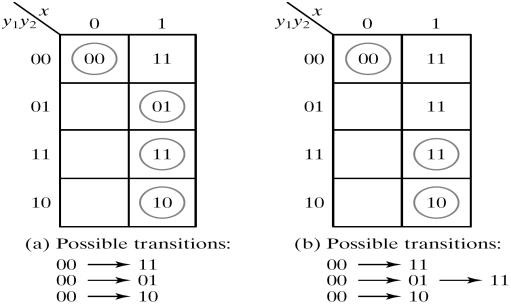
1. **What is lockout? How is avoided?**

Lockout condition is that condition wherein a counter gets onto a forbidden state and rather than coming out of it to another acceptable state or initial state, the counter switches to another forbidden state and gets stuck up in the cycle of forbidden states only.

The counter should be provided with an additional circuit. This will force the counter from an unused state to the next state as initial state. It is not always necessary to force all unused states into an initial state. This frees the circuit from the Lock out condition.

1. **What is critical race condition? Give example.**

A *critical race condition* occurs when the order in which internal variables are changed determines the eventual state that the state machine will end up in.



1. **Difference between synchronous and asynchronous sequential circuits.**

|  |  |  |
| --- | --- | --- |
| **S.No** | **Synchronous sequential circuits** | **Asynchronous sequential circuits** |
| 1 | The change of internal state occurs in  response to a clock pulse. | The change in internal state occurs whenever there is a change in input  Variable. |
| 2 | Memory elements are clocked flip-flops | Memory elements are unclocked flip-flops  or Time delay units. |
| 3 | The present state is totally specified by  FF values and does not change if input changes while clock pulse is inactive | There is no clock pulse. Because of  absence of clock, asynchronous circuits are faster than synchronous circuits. |
| 4 | Design is easy. | Design is more difficult because of the timing problems involved in the feedback path. |

1. **What is a Hazard?**

Hazards are unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays. Hazards occur in combinational circuits, where they may cause a temporary false output value. When this condition occurs in asynchronous sequential circuits, it may result in a transition to a wrong stable state. Steps must be taken to eliminate this effect.

1. **Difference between fundamental mode circuits and pulse-mode circuits.**

**Fundamental Mode Circuit**

1. The input variables change only when the circuit is stable.
2. Only one input variable can change at a given time
3. Inputs are levels and not pulses.

**Pulse Mode Circuits**

1. The input variables are pulses instead of levels.
2. The width of the pulses is long enough for the circuit to respond to the input.

The pulse width must not be so long that it is still present after the new state is reached and cause a faulty change of state.(iv) No two pulses should arrive at the input lines simultaneously.

1. **What are cycles and races?**

A cycle occurs when an asynchronous circuit makes a transition through a series of unstable states. If a cycle does not contain a stable state, the circuit will go from one unstable to stable to another, until the inputs are changed. When 2 or more binary state variables change their value in response to a change in an input variable, race condition occurs in an asynchronous sequential circuit. In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.

1. **What are the different types of shift type?**

There are five types. They are,

(i) Serial In Serial Out Shift Register (ii) Serial In Parallel Out Shift Register

(iii) Parallel In Serial Out Shift Register (iv) Parallel In Parallel Out Shift Register

1. **What do you mean by Race condition?**

A race condition is said to exist in an asynchronous sequential circuit when two or more binary state variables change value in response to a change in an i/p variable. When unequal delays are encountered, a race condition may cause the state variables to change in an un predictable manner.

1. **Differentiate Static & Dynamic Hazard.**

**Static 1-hazard:** The output may momentarily go to 0 when it should remain.

**Static 0-hazard:** The output may momentarily go to 1 when it should remain 0.

**Dynamic hazard** causes the output to change three or more times when it should change from 1 to 0 or from 0 to 1

1. **What is ASM chart?**

i) Algorithmetic State Machine (ASM) chart is a special type of flow chart suitable for describing the sequential operation in a digital system. (ii)A state machine is another term for a sequential circuit, which is the basic structure of a digital system. (iii) The ASM chart is composed of three basic elements: the state box, the decision box and the conditional box.

1. **What is State Assignment?**
2. Assigning binary values to each state that is represented by letter symbol in the

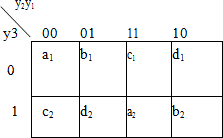
flow table of sequential circuit is called state assignment.

1. The primary objective in choosing a proper binary state assignment in asynchronous circuit is the prevention of critical races.
2. **Define Essential Hazard.**

An essential Hazard is caused by unequal delays along two or more paths that originate from the same input. An excessive delay through an inverter circuit in comparison to the delay associated with the feedback path may cause such a hazard. Essential hazards cannot be corrected by adding redundant gates as in static hazards. To avoid essential hazard, each feedback loop must be handled with individual care to ensure that the delay in the feedback path is long enough compared to delays of other signals that originate from the input terminals.

1. **Explain Multiple row method.**

In the multiple row assignment each state in the original flow table is replaced by two or more combinations of state variables. The state assignment map shows the multiple row assignment that can be used with any four- row flow table.



1. **Define closed covering.**

The condition that must be satisfied for row merging is that the set of chosen compatibles must cover all the states that must be closed. The set will cover all the states if it includes all the states of the original state table. The closure condition is satisfied if there are no implied states or if the implied states are included within the set. A closed set of compatibles that covers all the states is called a closed covering.